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SYNTHESIS OF LOW POWER FSM USING CLOCK GATING TECHNIQUE

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Abstract **- Power dissipation has become a key concern for circuit designers when developing an integrated circuit as chip sizes have diminished with the advent of technology. Static and dynamic power is significant sources of power dissipation. A serial adder, one among the crucial paths of any processor micro architecture, suffers to huge power flow. In this paper, we have come up with a technique to generate carry out of serial adder using clock gating approach.**

Index Terms ***–Integrated circuits, Serial Adder, Clock gating.***

I. INTRODUCTION

The evolution of low power application in integrated circuits with expanding operating frequency has compelled the quest for intelligent power reduction strategies. According to the International Technology Roadmap for Semiconductors (ITRS) report from 2013, the increment in clock frequencies and chip density, as well as the integration of different technological advances in a tiny space (tablets, phablets, and GPS, for example), has transitioned the VLSI industry's engagement from speed to low power [1]. In recent days, the vigorous downscaling of process technologies has introduced the use of devices like tablet PCs and smart phones. To sustain the virtue of mobility, the majority of these gadgets employ dependable micro-architectures with relatively low power consumption. Serial adders are one of the most ubiquitous power-hungry micro-architectures, with their 'SUM' output reliant on the preceding 'CARRY' output, which is serially stored in a bit storage cell as depicted in the figure 1.

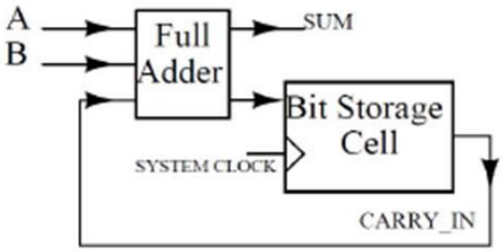

Fig 1: Block level view of Serial Adder

For initial storage, data register packs composed of flip flops are used for inputs A, B, and output 'SUM'. The data register is used for partial sums which occur during the addition operation. Despite the fact that both parallel and serial adders have identical peripheral overheads, serial adders require only a single full adder for multi-bit addition, whereas parallel adders require multiple full adders. Serial adders are typically favoured over parallel adders because they require fewer moving parts to obtain the desired output [2]. The static power emanating from leakage current through active and inactive devices, as well as the dynamic power emanating from the clock switching transitions triggering the sequential block, are the two key aspects of serial adder power consumption [3]. Power gating is a notion which can be used to restrict the contention current [4]. The circuit network is coupled to the power supply through sleep transistors, which are regulated transistors. These sleep transistors regulate current flow in the circuit network, limiting it only during active periods. Furthermore, the addition of sleep transistors reduces the logic value of the power supply voltage. As a result, power gating is not the better way. Switching power, on the other hand, is a major concern for dynamic power dissipation, though it is regulated by the clock-net in the circuit network. When no operation is performed, the clock signal is left off for a period of time to resolve the problem. As a result, the design's switching activity factor is decreased, resulting in substantial dynamic power reduction. This technique is referred as Clock

Gating technique [5]. As a result, the most effective solution to this problem is to incorporate an efficient clock gating mechanism into the serial adder design, which may prevent current leakage via the power lines and decrease clock signal transitions while the input data to the sequential element remains constant. In this paper, we have implemented the efficient clock gating technique for carry signal of the serial adder [6].

The following is the structure of the paper: We briefly discuss the different clock gating strategies and the design of the serial adder in section II. The theory of operation of the clock gating method is described in Section III. In Section IV, the serial adder finite state machine (FSM) and its implementation utilizing clock gating method are described. Section V compares one approach to another with a different clock gating strategy.

II. LITERATURE SURVEY

Latch free based gating, latch-based gating, and flip-flop-based gating are the three types of clock gating approaches. Each of the three groups has benefits and drawbacks which are extensively discussed in [7]. A few additional gating approaches have been developed by merging latch-free and latch-based gating types. According to the study, these are double-gated gating, NC2MOS gating, dynamic gating, and bootstrap XOR gating as depicted in [8], [9] and [10]. This paper concentrates on serial adder design since they are a key component of current CPU microarchitectures and consume a lot of power. Serial adders are also the ideal option for creating multi-bit binary adders if operational speed is not a factor, because they have the least overhead compared to other adders. Different 1-bit serial adder design approaches have been described in [11]. However, when modelled on 0.8m technology with a 2.4Volt power supply, the greatest and least average power required by those devices are 13Watt and 4.39Watt respectively. We were inspired to create this since low power application is a contemporary need in CPU designs. As a result, an attempt is made to use the clock gating (CG) strategy in the serial adder design since it has a vast capability to reduce static power dissipation

III. CLOCK GATING TECHNIQUE

The key factors to power consumption, as outlined in section 1, are static and dynamic power dissipation. Even when a CMOS circuit is turned off, some static power waste occurs due to leakage current through nominally off transistors. In CMOS logic gates, both nMOS and pMOS transistors exhibit finite reverse leakage and sub-threshold currents. The overall power dissipation owing to leakage current is comparable to dynamic power dissipation in a silicon chip with millions of transistors. Processing factors influence the values of leakage and sub-threshold currents. We will solely look at dynamic power consumption in this paper.

In a CMOS circuit, dynamic power dissipation is only consumed when switching activity occurs at particular nodes. For example, a chip may have a large number of capacitive nodes, but if the circuit does not switch, no dynamic power is consumed. Equation for dynamic power dissipation is given below $\mathbf{P_{dyn}= C_L V_{DD}^2 f}$, where C_L is the total capacitance seen at the output and f is the signal frequency and is given by $\mathbf{f= \alpha * f_{clk}}$ where f_{clk} is the system frequency.

Clock elements are the most common switching elements in digital VLSI designs. Clock switching power could account for up to 50% of total power in some designs. The principle behind clock gating is to stop the clock of those sequential elements whose data is not toggling. Only data flow is

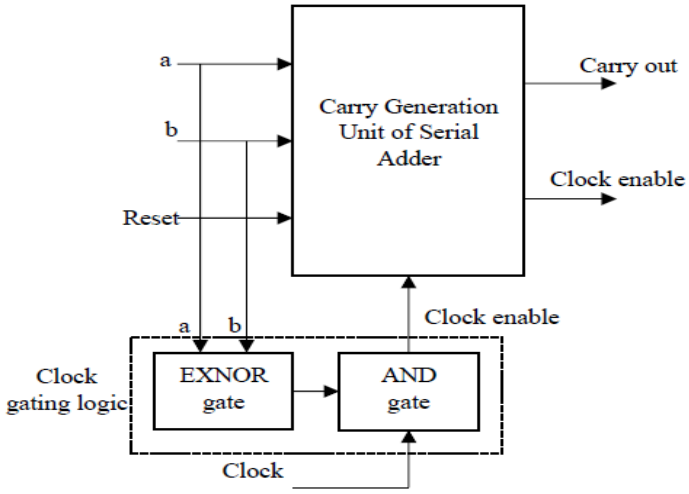

Fig 2: Block level view of Clock Gated Carry Generation Circuit

discussed at the RTL level. The clock can have a condition that prevents a flip-flop from switching its output if that condition is fulfilled. This is accomplished by employing the clock enable signal, which is dependent on both the system

clock signal and the inputs. In this study, we identified conditions in which the clock does not need to reach the carry generation circuit of a 4-bit serial adder, i.e., scenarios in which the serial adder's carry output does not change. In this paper, we have designed a logic for the same using fundamental logic gates which is shown in the figure 2 below.

IV. FINITE STATE MACHINE FOR CARRY OUT

The FSM, which is a type of abstraction, is used to model the behavior of any digital system by indicating each available state and the related transition between states. A Finite State Machine (FSM) is a machine that has a collection of states, a start state, an input, and a transition function that transfers input and current states to the next state. With an input, the machine enters the start state. Depending on the transition function, it switches to new states. The transition function is influenced by current inputs and states. The machine's output is determined by its input and/or present state.

In digital design, there are two types of FSMs that are commonly employed. They are:
1) Moore machine.
2) Mealy machine.

A serial adder is a digital system that combines a full adder and a flip-flop to calculate the addition of two arbitrary values. Bitwise addition is performed on the full adder from the least significant bit (LSB) to the most significant bit (MSB) for multi bit addition operations. Sum and carry are generated by bitwise addition. From LSB to MSB, this carry is transmitted and added bit by bit. Therefore, the carry is considered as a state variable. The value of the state variable carry can be either binary ‘0' or binary ‘1’. State ‘A' corresponds to binary ‘0,' while state ‘B' corresponds to binary ‘1’. Figure 3 shows the Moore model for the carry generation of serial adder with the output carry, which is dependent on the state variable A (corresponds to carry '0') and B (corresponds to carry '1').

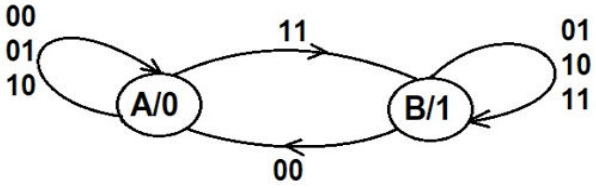

Fig 3: FSM of Carry Generation circuit

Table 1: State Table for Carry Generation Logic

Present state	Input (a[n], b[n])	Next state	Output
A	00	A	0
A	01	A	0
A	10	A	0
A	11	B	1
B	00	A	0
B	01	B	1
B	10	B	1
B	11	B	1

The state transition occurs depending on the input a and b. From the FSM it is observed that the state variable does not change when both the inputs to the FSM are different. The transitions from one state to another state occur only when both the inputs are same (00 or 11). Figure 3 depicts this fact using a state diagram. This behavior of the design is utilized to turn off the clock when the state need not change. Thus, reducing the switching activity which in turn reduces the dynamic power consumption. Whenever the current state is A (carry 0) and the input combinations are 00, 01, or 10, the state does not change; it stays in A. Only when the inputs are 11 it will go from state A to state B. Similarly, if the current state is B (carry 1) and the input combinations are 11, 01, or 10, the state will not change; it will remain B. Only when the inputs are 00 it will switch from state B to A.

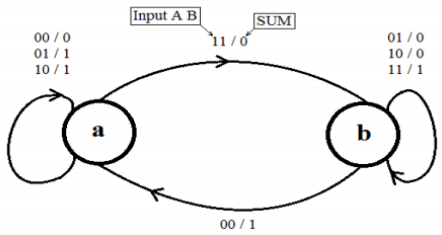

Fig.4: State Diagram of Mealy FSM for Serial Adder

Figure 4 shows the Mealy model for the serial adder with the output ‘SUM,' which is dependent on the state variable ‘CARRY IN' as well as the current input values A and B.

V. RESULTS

The suggested architecture is designed using Verilog Hardware Description Language (HDL). The behavioral description has been written for this design and Xilinx ISE

14.7 is used for simulation of the model. The functionality of the design has been tested and verified. The serial adder is also tested by incorporating both the designed carry out sequential element which uses the gated clock and also by using a normal circuit which does not use any gating technique. It has been observed that the power dissipation is less in the circuit which uses the clock gating technique as compared to the traditional carry generation circuit. The simulation results is shown in the figure 5 given below.

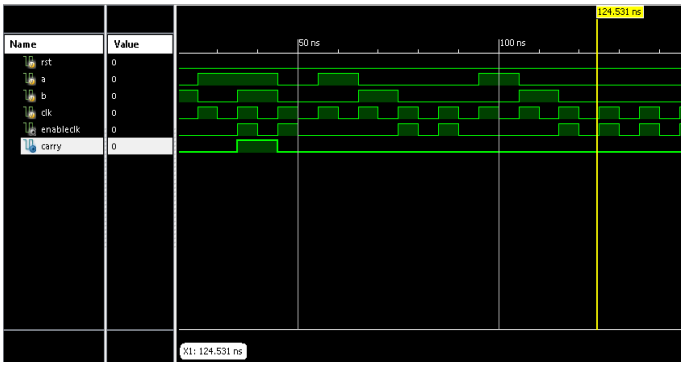

Fig.5: Simulation Results

The design is synthesized using Xilinx XST. The RTL schematic of the designed carry generation circuit using clock gating technique is provided in the figure 6.

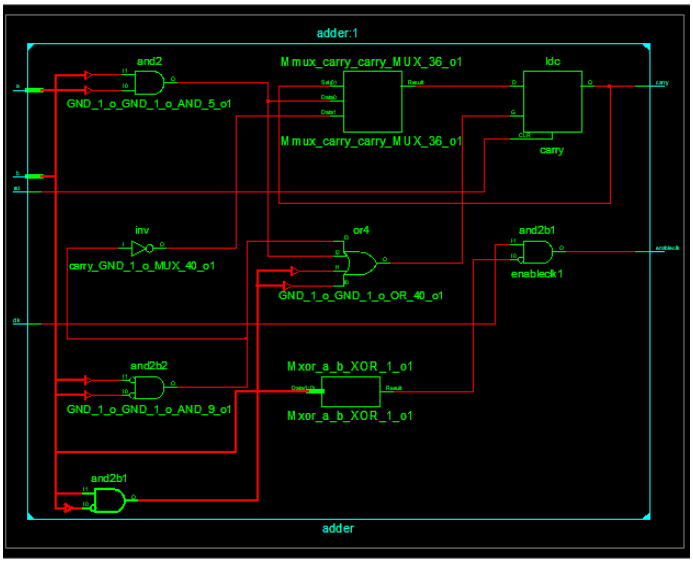

Fig 6: RTL Schematic of carry generation circuit

The power reports obtained for both the serial adder design shows that the average power consumed by the serial adder implemented using clock gating technique is less compared to the normal approach. The power analysis is shown in table 2 given below.

Table 2: Power Analysis

Design	Dynamic Power (µW)	Average Power (µW)
Serial adder with gated clock	69.6	142.45
Normal serial adder	78.96	160.25

VI. Conclusion

The performance of the proposed design has been reviewed in terms of simulation results, illustrating that the proposed method is superior in terms of power usage. The same has been synthesized using Xilinx XST and the RTL Schematic and the power reports has been obtained.

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